A LOW POWER AND RECONFIGURABLE ADAPTIVE FIR FILTER IN MULTIPLIERS

R.RUBY, ME (VLSI DESIGN),

M.JAYAKUMAR,ASSISTANT PROFESSOR,ECE

Department of Electronics and Communication, Sengunthar Engineering College, Affiliated to Anna University, Tiruchengode

rubijayaprakash@gmail.com

ABSTRACT: *The explosive growth in mobile computing and portable multimedia applications has increased the demand for low power digital signal processing (DSP) systems. One of the most widely used operations performed in DSP is finite impulse response (FIR) filtering. This project gives an architectural approach to the design of low power reconfigurable finite impulse response (FIR) filter. The approach is well suited when the filter order is fixed and not changed for particular applications, and efficient trade-off between power savings and filter performance can be made using the proposed architecture. Generally, FIR filter has large amplitude variations in input data and coefficients. Considering the amplitude of the filter coefficients and inputs, the proposed FIR filter dynamically changes the filter order. Mathematical analysis on power savings and filter performance degradation and its experimental results show that the proposed approach achieves significant power savings without seriously compromising the filter performance. The power savings is up to 41.9% with minor performance degradation and the area overhead of the proposed scheme is less than 5.3% compared to the Conventional approach.*

I. INTRODUCTION

The explosive growth in mobile computing and portable multimedia applications has increased the demand for low power digital signal processing (DSP) systems. One of the most widely used operations performed in DSP is finite impulse response (FIR) filtering. The input-output relationship of the linear time invariant (LTI) FIR filter can be expressed as the following equation:

$$Y(n) = \sum_{n=0}^{N-1} c_k x(n-k) \qquad (1)$$

In many applications, in order to achieve high spectral containment and/or noise attenuation, FIR filters with fairly large number of taps are necessary. Many previous efforts for reducing power consumption of FIR filter generally focus on the optimization of the filter coefficients while maintaining a fixed filter order. In those approaches, FIR filter structures are simplified to add and shift operations, and minimizing the number of additions/subtractions is one of the main goals of the research. However, one of the drawbacks encountered in those approaches is that once the filter architecture is decided, the coefficients cannot be changed; therefore, those techniques are not applicable to the FIR filter with programmable coefficients. Approximate signal processing techniques are also used for the design of low power digital filters. In filter order dynamically varies according to the stop band energy of the input signal.

However, the approach suffers from slow filter-order adaptation time due to energy computations in the feedback mechanism. Previous studies in show that sorting both the data samples and filter coefficients before the convolution operation has a desirable energy-quality characteristic of FIR filter. However, the overhead associated with the real-time sorting of incoming samples is too large. Reconfigurable FIR filter architectures are previously proposed for low power implementations or to realize various frequency responses using a single filter. For low power architectures, variable input word-length and filter taps , different coefficient word-lengths , and dynamic reduced signal representation techniques are used. In those works, large overhead is incurred to support reconfigurable schemes such as arbitrary nonzero digit assignment or programmable shift. In this paper, we propose a simple yet efficient low power reconfigurable FIR filter architecture, where the filter order can be dynamically changed depending on the amplitude of both the filter coefficients and the inputs. In other words, when the data sample multiplied to the coefficient is so small as to mitigate the effect of partial sum in FIR filter, the multiplication operation can be simply cancelled. The filter performance degradation can be minimized by controlling the error bound as small as the quantization error or signal to noise power ratio (SNR) of given system. The primary goal of this work is to reduce the dynamic power of the FIR filter, and the main contributions are summarized as follows. 1) A new reconfigurable FIR filter architecture with real-time input and coefficient monitoring circuits is presented. Since

the basic filter structure is not changed, it is applicable to the FIR filter with programmable coefficients or adaptive filters. 2) We provide mathematical analysis of the power saving and filter performance degradation on the proposed approach. The analysis is verified using experimental results, and it can be used as a guideline to design low power reconfigurable filters. The rest of the paper is organized as follows. In Section II, the basic idea of the proposed reconfigurable filter is described. Section III presents the reconfigurable hardware architecture and circuit techniques used to implement the filter. Discussions on the design considerations and mathematical analysis of the proposed reconfigurable FIR filter are presented in Section IV. Section V shows the numerical results, followed by conclusions in Section VI.

II. Reconfigurable FIR Filtering to Trade Off Filter Performance and Computation Energy

As shown in Fig. 1, FIR filtering operation performs the weighted summations of input sequences, called as convolution sum, which are frequently used to implement the frequency selective—low-pass, high-pass, or band-pass—filters. Generally, since the amount of computation and the corresponding power consumption of FIR filter are directly proportional to the filter order, if we can dynamically change the filter order by turning off some of multipliers, significant power savings can be achieved. However, performance degradation should be carefully considered when we change the filter order.

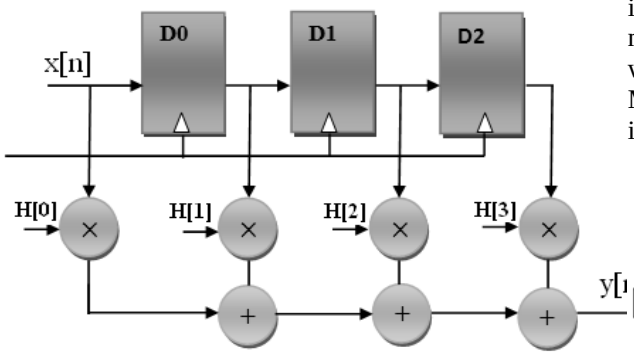


Fig.1Typical Direct form of FIR filter

Therefore, the basic idea is that if the amplitudes of both the data input and filter coefficient are small, the multiplication of those two numbers is proportionately small; thus, turning off the multiplier has negligible effect on the filter performance. For example, since two's complement data format is widely used in the DSP applications, if one or both of the multiplier input has negative value, multiplication of two small values gives rise to large switching activities, which is due to the series of 1's in the MSB part. By cancelling the multiplication of two small numbers, considerable power savings can be achieved with negligible filter performance degradation. In the fixed point arithmetic of FIR filter, full operand bit widths of the multiplier outputs is not generally used. In other words, as shown in Fig. 1, when the bit-widths of data inputs and coefficients are 16, the multiplier generates 32-bit outputs. However, considering the circuit area of the following adders, the LSBs of multipliers outputs are usually truncated or rounded off, (e.g., 24 bits are used in Fig. 1) which incurs quantization errors. When we turn off the multiplier in the FIR filter, if we can carefully select the input and coefficient amplitudes such that the multiplication of those two numbers is as small as the quantization error, filter performance degradation can be made negligible.

III. Architecture of Reconfigurable FIR Filter

In this section, we present a direct form (DF) architecture of the reconfigurable FIR filter, which is shown in Fig. 3 In order to monitor the amplitudes of input samples and cancel the right multiplication operations, amplitude detector (AD) in Fig. 3 is used. Dynamic power consumption of CMOS logic gates is a strong function of the switching activities on the internal node capacitances. In the proposed reconfigurable filter, if we turn off the multiplier by considering each of the input amplitude only, then, if the amplitude of input x(n) abruptly changes for every cycle, the multiplier will be turned on and off continuously, which incurs considerable switching activities. Multiplier control signal decision window (MCSD) in Fig. 3(a) is used to solve the switching problem.

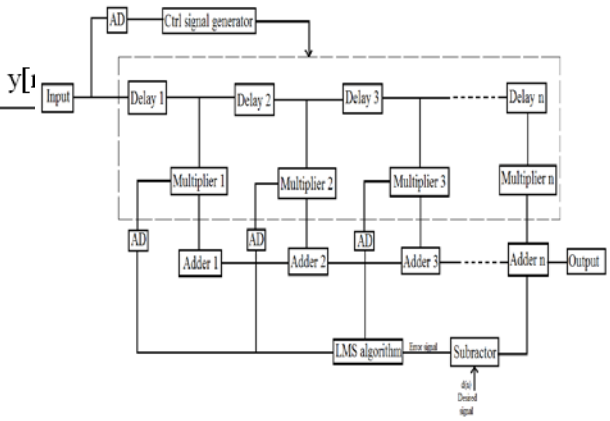


Fig. 3 Proposed reconfigurable FIR filter architecture.

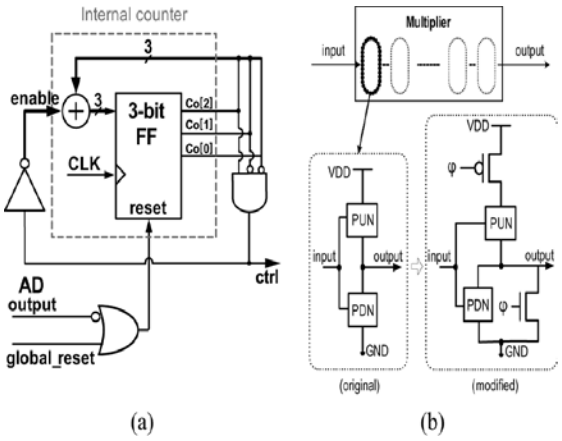


Fig. 4. (a) Schematic of *ctrl* signal generator. Internal counter sets ctrl signal to "1" when all input samples inside MCSD are smaller than Xth (m=4case). (b) Modified gate schematic to turn off multiplier.

Fig. 4(a) shows the *ctrl* signal generator design. As an input smaller than Xth comes in and AD output is set to "1", the counter is counting up. When the counter reaches m , the *ctrl* signal in the figure changes to "1", which indicates that m consecutive small inputs are monitored and the multipliers are ready to turn off.

IV. Design Considerations and Mathematical Analysis on the Reconfigurable FIR Filter

In this section, we present design considerations on the proposed reconfigurable FIR filter. Mathematical analysis which describes the trade-off between power savings and filter performance degradation is also presented in this section.

A. Design Considerations

In following discussions, as a metric of power savings, we use the power consumption ratio, , which means the ratio of the reconfigurable filter power consumption to the conventional filter power . As a measure of filter performance degradation, we use mean-square error (MSE) between the proposed reconfigurable filter output and original filter output. The most important factors that have a large effect on the proposed filter performance and power consumption are and. When and are set too large, it can give rise to large power savings with considerable distortion in the filter output. On the other hand, if and are too small, power savings become trivial. The other one to be considered is , the length of MCSD. Fig. 5 shows the number of input samples whose (axis) consecutive input values are smaller than input threshold. The input signals used in the simulation are more than ten samples of sounds and speeches.

In Fig. 5, if we choose a specific value in the axis, the total number of cancelled multiplications is the accumulated number of samples from the selected value to the right. Therefore, if m becomes larger, the number of input samples that make multipliers turned off decreases; then, power reduction becomes smaller and filter performance degradation becomes lower as well.

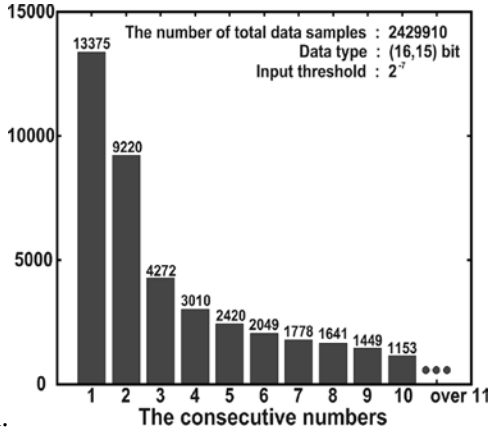


Fig. 5. Number of consecutive input samples whose amplitudes are smaller than Xth in sound and speech signals.

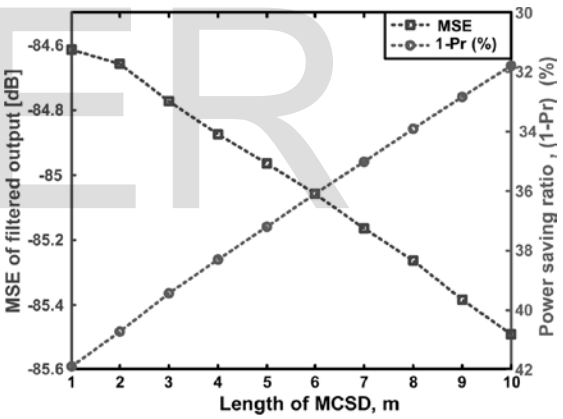


Fig.6. Power saving ratio versus performance degradation percentage change for different MCSD length, _ in the case of 75-tap equip-ripple filter.

B. Mathematical Analysis

Mathematical modelling on the power savings and performance degradation of the proposed reconfigurable FIR filter are presented in this subsection.

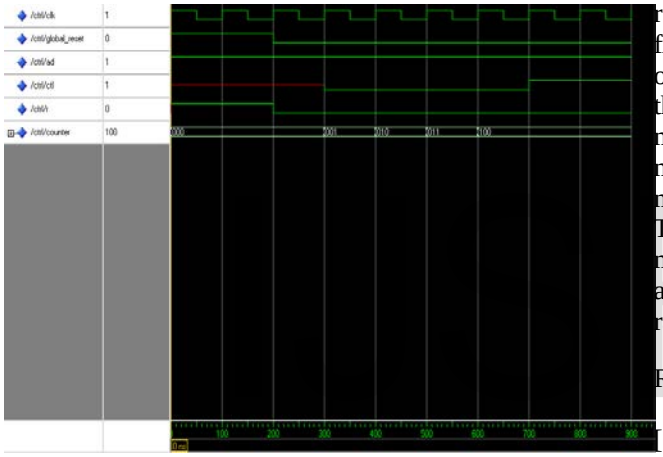
V. SIMULATION RESULTS

A.CONTROL SIGNAL GENERATOR

As an input smaller than Xth comes in and AD output is set to "1", the counter is counting up. When the counter reaches, the *ctrl* signal in the

figure changes to "1", which indicates that consecutive small inputs are monitored and the multipliers are ready to turn off. One additional bit, in_{ct_n}, is added and it is controlled by *ctrl*. The in_{ct_n} accompanies with input data all the way in the following flip-flops to indicate that the input sample is smaller than **X**th and the multiplication can be canceled when the coefficient of the corresponding multiplier is also smaller than **C**th. Once the signal in_{ct_n} is set inside MCSD, the signal does not change outside MCSD and holds the amplitude information of the input. A delay component is added in front of the first tap for the synchronization between $x^*(n)$ and in_{ct_n}since one clock latency is needed due to the counter in MCSD.

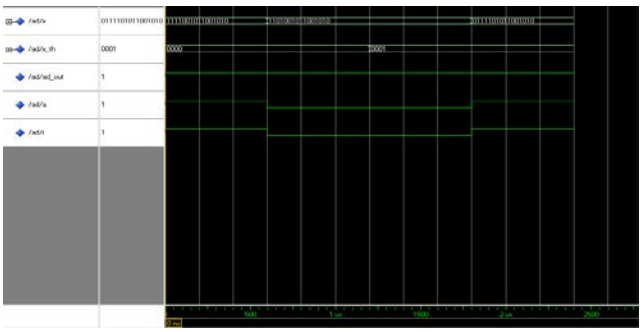
OUTPUT WAVEFORM FOR CTRL SIGNAL GENERATOR



B.AMPLITUDE DETECTION LOGIC

In case of adaptive filters, additional ADs for monitoring the coefficient amplitudes are required. However, in the FIR filter with fixed or programmable coefficients, since we know the amplitude of coefficients ahead, extra AD modules for coefficient monitoring are not needed. The coefficients of a typical 25-tap low-pass FIR filter The central coefficient has the largest value the coefficient has the largest value in the 25-tap FIR filter and the amplitude of the coefficients generally decreases as becomes more distant from the center tap. The data inputs of the filter, which are multiplied with the coefficients, also have large variations in amplitude. Therefore, the basic idea is that if the amplitudes of both the data input and filter coefficient are small, the multiplication of those two numbers is proportionately small; thus, turning off the multiplier has negligible effect on the filter performance.

OUTPUT WAVEFORM FOR AD LOGIC



VI. CONCLUSION

This project gives the study of propose low power reconfigurable FIR filter architecture where the filter order can be dynamically changed depending on the amplitude of both the filter coefficients and the inputs. In other words, when the data sample multiplied to the coefficient is so small as to mitigate the effect of partial sum in FIR filter, the multiplication operation can be simply canceled. The filter performance degradation can be minimized by controlling the error bound as small as the quantization error or signal to noise power ratio (SNR) of given system.

REFERENCES

[1] H. Samueli, "An improved search algorithm for the design of multiplier less FIR filter with powers-of-two coefficients," *IEEE Trans. Circuits Syst.*, vol. 36, no. 7, pp. 1044–1047, Jul. 1989.
[2] R. I. Hartley, "Subexpression sharing in filters using canonical signed digit multipliers," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 43, no. 10, pp. 677–688, Oct. 1996.
[3] O. Gustafsson, "A difference based adder graph heuristic for multiple constant multiplication problems," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2007, pp. 1097–1100.
[4] S. H. Nawab, A. V. Oppenheim, A. P. Chandrakasan, J. M. Winograd, and J. T. Ludwig, "Approximate signal processing," *J. VLSI Signal Process.*, vol. 15, no. 1–2, pp. 177–200, Jan. 1997.
[5] J. Ludwig, H. Nawab, and A. P. Chandrakasan, "Low power digital filtering using approximate processing," *IEEE J. Solid-State Circuits*, vol. 31, no. 3, pp. 395–400, Mar. 1996.
[6] A. Sinha, A. Wang, and A. P. Chandrakasan, "Energy scalable system design," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 10, no. 2, pp. 135–145, Apr. 2002.
[7] K.-H. Chen and T.-D. Chiueh, "A low-power digit-based reconfigurable FIR filter," *IEEE Trans.*

Circuits Syst. II, Exp. Briefs, vol. 53, no. 8, pp. 617–621, Dec. 2006.
[8] R. Mahesh and A. P. Vinod, "New reconfigurable architectures for implementing filters with low complexity," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 29, no. 2, pp. 275–288, Feb. 2010.
[9] Z. Yu, M.-L. Yu, K. Azadet, and A. N. Wilson, Jr, "A low power FIR filter design technique using dynamic reduced signal representation," in *Proc. Int. Symp. VLSI Tech., Syst., Appl.*, 2001, pp. 113–116.
[10] R. Mahesh and A. P. Vinod, "Coefficient decimation approach for realizing reconfigurable finite impulse response filters," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2008, pp. 81–84.
[11] J. Park and K. Roy, "A low complexity reconfigurable DCT architecture to trade off image quality for power consumption," *J. Signal Process. Syst.*, vol. 53, no. 3, pp. 399–410, Dec. 2008.
[12] J. G. Proakis, *Digital Communications*, 3rd ed. New York: McGraw- Hill, 1995. [13] Synopsys, Inc., Nanosim Reference Guide, 2007.
[14] S. Hwang, G. Han, S. Kang, and J. Kim, "New distributed arithmetic algorithm for low-power FIR filter implementation," *IEEE Signal Process. Lett.*, vol. 11, no. 5, pp. 463–466, May 2004.
[15] A. L. Garcia, *Probability, Statics, and Random Processes for Electrical Engineering*. Upper Saddle River, NJ: Pearson Education, 2009.